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# FOUR DUAL DIODES (FDD-1A) MODULE P/N 841559

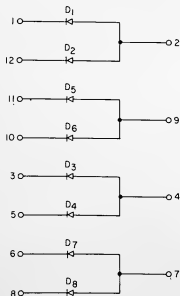
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## Functional Description

The Four Dual Diodes, FDD-1A, module consists of four pairs of two diodes with common anodes between pairs. The common anodes and individual cathodes are terminated at the module pins thereby offering the circuit designer uniformity of circuit packaging as well as flexibility in application with other SLT modules. In addition, each pair of diodes can be used in applications where diodes with matched characteristics are required.

## Schematic



## Terminal Configuration



TOP VIEW

 Mechanical  
Chamfer  
Right Side

## Maximum Ratings

Maximum Current = 25ma

Breakdown Voltage = 13V

## FDD-1A Module Functional Tests

INDIVIDUAL DEVICE PARAMETER TESTS					
TESTS	COM- PONENTS	TEST CONDITIONS	T °C	LIMITS	
				MIN	MAX
$Q_S$	$D_1 - D_2$	$I_F = 3.0ma$ , See Fig. 1	25		PC
$V_F$	$D_1 - D_2$	$I_F = 2.0ma$ , See Fig 2	25		0.25 V
$V_F$	$D_1 - D_2$	$I_F = 0.1ma$	25	0.51	V
$V_F$	$D_1 - D_2$	$I_F = 0.5ma$	25	0.58	V
$V_F$	$D_1 - D_2$	$I_F = 1.0ma$	25	0.61	V
$V_F$	$D_1 - D_2$	$I_F = 2.0ma$	25	0.64	V
$V_F$	$D_1 - D_2$	$I_F = 5.0ma$	25	0.87	V
$V_F$	$D_1 - D_2$	$I_F = 15ma$	25	1.05	V
$V_F$	$D_1 - D_2$	$I_F = 25ma$	25	0.83	1.10 V
$I_{Fk}$	$D_1 - D_2$	$I_k = 10\mu a$	25	13	V
$I_k$	$D_1 - D_2$	$V_E = 12V$	75	0.3	μa
DIODE CAPACITANCE	$D_1 - D_2$	OV BIAS, $f = 1 \pm 0.5mhz$ AC SIGNAL $\leq 50mv$ P-P	25		3.3 pf

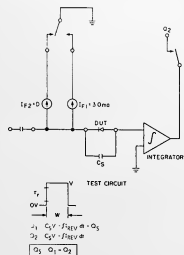


FIGURE 1

## Notes

For this test the diode shunt capacity (incl Probe) shall be  $10.5 \pm 1$  pf with a 50Ω HF Resistor in place of the Diode, the rise time,  $t_r$ , of the input voltage wave form shall be  $\leq 2$  ns, the operating frequency  $\leq 50KHz$ , pulse width  $\leq 50ns$ , Bandwidth of detector  $\geq 750MHz$ . Turn on is from  $V_F = 0$ .

## Store Charge Test

$V$ -PULSE AMPLITUDE:  $5V \pm 25\%$

$W$ -PULSE WIDTH:  $\rightarrow 50ns$

RISE TIME:  $1\% - 50\% < 0.5ns$

$10\% - 90\% < 0.4ns$

SOURCE IMPEDANCE  $< 10$  OHMS

$I_{F1}$  -FORWARD CURRENT =  $3.0ma \pm 0.3\%$

$I_{F2}$  -FORWARD CURRENT =  $0ma$

$C_S$  - SHUNT CAPACITY  $< 50$  pf

INTEGRATOR RESPONSE  $\leq 1ns$

$Q_1$  -CHARGE WHEN  $D, U, T, IS$  FORWARD

BIASED WITH  $I_{F1} = 3.0ma$

$Q_2$  -CHARGE WHEN  $D, U, T, IS$  FORWARD

BIASED WITH  $I_{F2} = 0ma$

$Q_3$  - STORED CHARGE

$I_{REV}$  -DIODE LEAKAGE CURRENT

## Forward Recovery

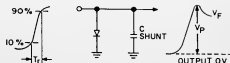


FIGURE 2